FAIRCHILD SEMICONDUCTOR®

February 2007

UniFET™

FDD3N40 / FDU3N40

400V N-Channel MOSFET

Features

- 2A, 400V, $R_{DS(on)}$ = 3.4Ω @V_{GS} = 10 V
- Low gate charge (typical 4.5 nC)
- Low C_{rss} (typical 3.7 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

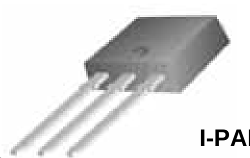
Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

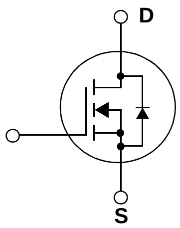
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



D-PAK
FDD Series



I-PAK
FDU Series



Absolute Maximum Ratings

Symbol	Parameter			FDD3N40 / FDU3N40	Unit
V_{DSS}	Drain-Source Voltage			400	V
I_D	Drain Current	- Continuous (T_C = 25°C) - Continuous (T_C = 100°C)		2.0 1.25	A A
I_{DM}	Drain Current	- Pulsed	(Note 1)	8.0	A
V_{GSS}	Gate-Source voltage			±30	V
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	46	mJ
I_{AR}	Avalanche Current		(Note 1)	2	A
E_{AR}	Repetitive Avalanche Energy		(Note 1)	3	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	4.5	V/ns
P_D	Power Dissipation	(T_C = 25°C) - Derate above 25°C		30 0.24	W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds			300	°C

* Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	4.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Case-to-Sink Typ.	--	110	°C/W

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD3N40	FDD3N40TM	D-PAK	380mm	16mm	2500
FDD3N40	FDD3N40TF	D-PAK	380mm	16mm	2000
FDU3N40	FDU3N40TU	I-PAK	-	-	70

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250μA	400	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	--	0.4	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 400V, V_{GS} = 0V V_{DS} = 320V, T_C = 125°C	-- --	-- --	1 10	μA μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30V, V_{DS} = 0V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30V, V_{DS} = 0V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10V, I_D = 1A	--	2.8	3.4	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40V, I_D = 1A (Note 4)	--	2	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	--	173	225	pF
C_{oss}	Output Capacitance		--	30	40	pF
C_{rss}	Reverse Transfer Capacitance		--	3.7	6	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 200V, I_D = 3A R_G = 25Ω (Note 4, 5)	--	10	30	ns
t_r	Turn-On Rise Time		--	30	70	ns
$t_{d(off)}$	Turn-Off Delay Time		--	10	30	ns
t_f	Turn-Off Fall Time		--	25	60	ns
Q_g	Total Gate Charge	V_{DS} = 320V, I_D = 3A V_{GS} = 10V (Note 4, 5)	--	4.5	6	nC
Q_{gs}	Gate-Source Charge		--	1.2	--	nC
Q_{gd}	Gate-Drain Charge		--	2	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	2	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	8	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0V, I_S = 2A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_S = 3A dI_F/dt =100A/μs (Note 4)	--	210	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.75	--	μC

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 20mH, I_{AS} = 2A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. $I_{SD} \leq$ 2A, di/dt $\leq$ 200A/μs, $V_{DD} \leq BV_{DSS}$, Starting T_J = 25°C
4. Pulse Test: Pulse width $\leq$ 300μs, Duty Cycle $\leq$ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

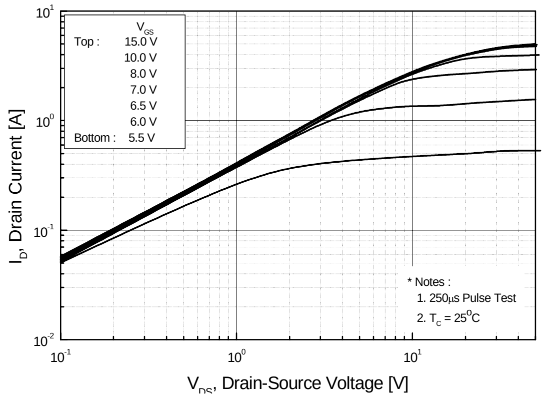


Figure 2. Transfer Characteristics

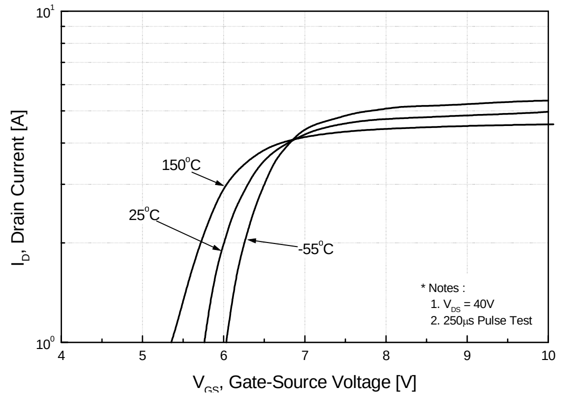


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

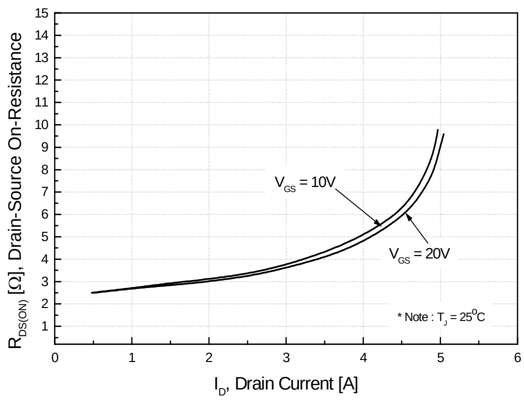


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperatue

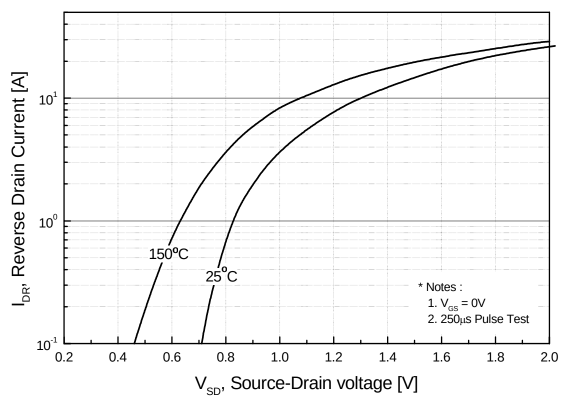


Figure 5. Capacitance Characteristics

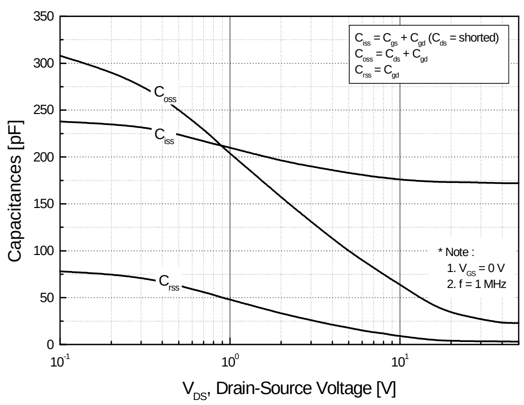
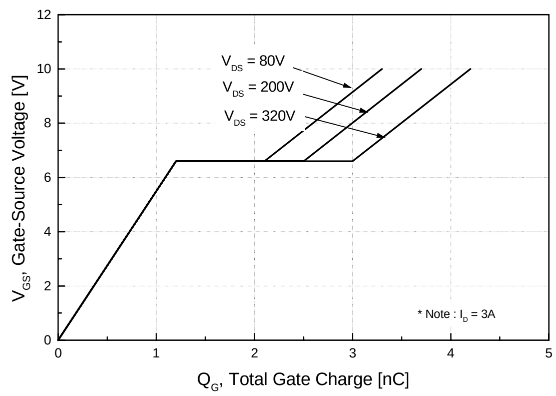


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

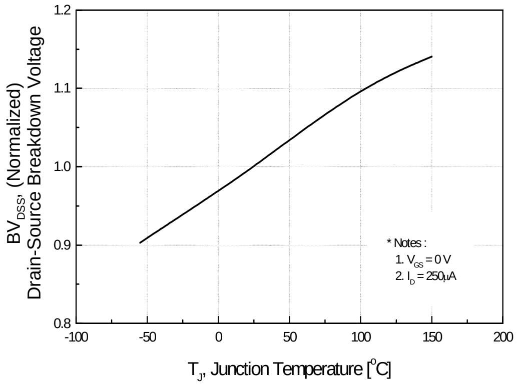


Figure 8. On-Resistance Variation vs. Temperature

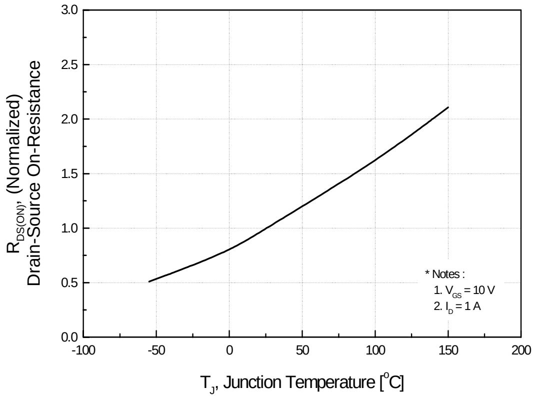


Figure 9. Maximum Safe Operating Area

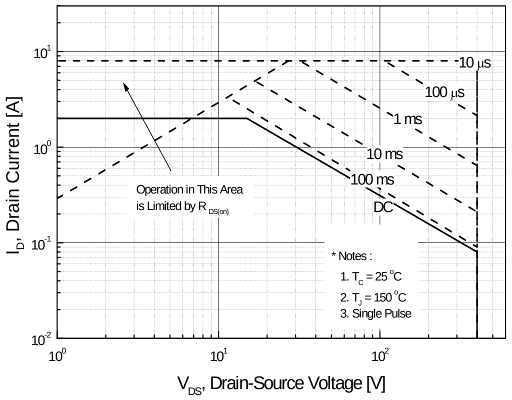


Figure 10. Maximum Drain Current vs. Case Temperature

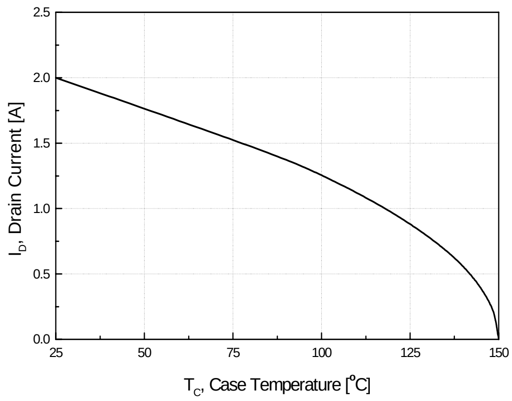
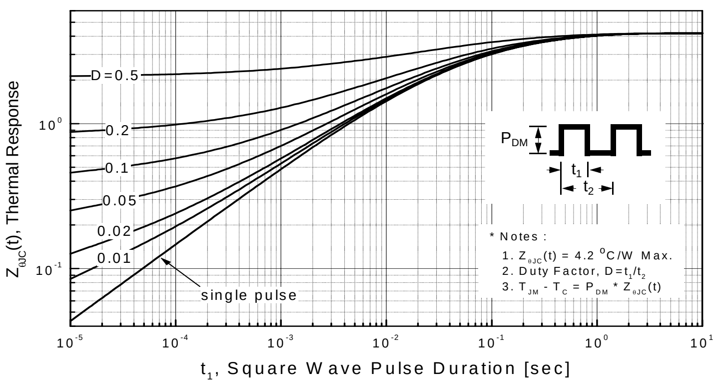
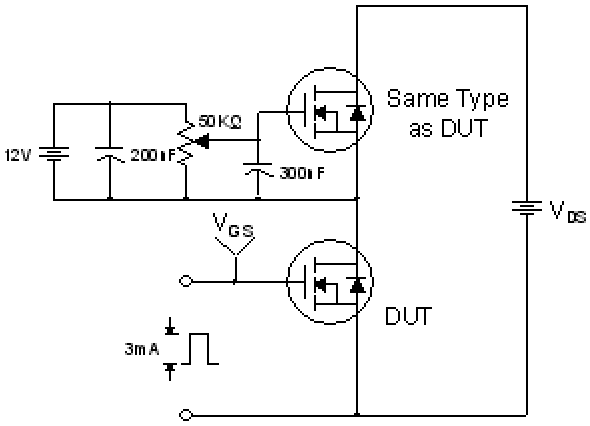
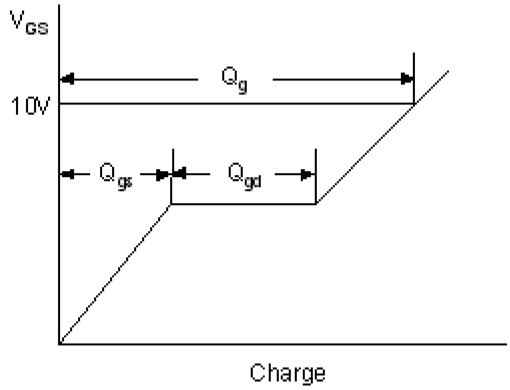


Figure 11. Transient Thermal Response Curve

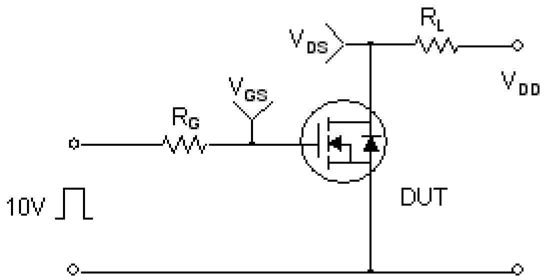


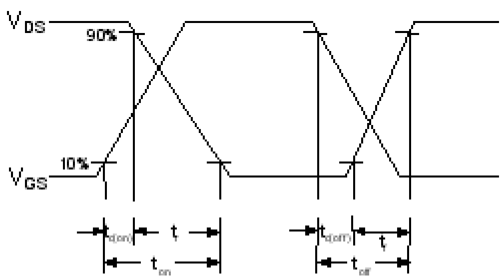
Gate Charge Test Circuit & Waveform



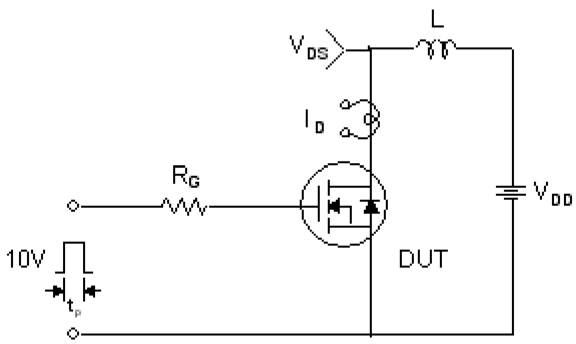


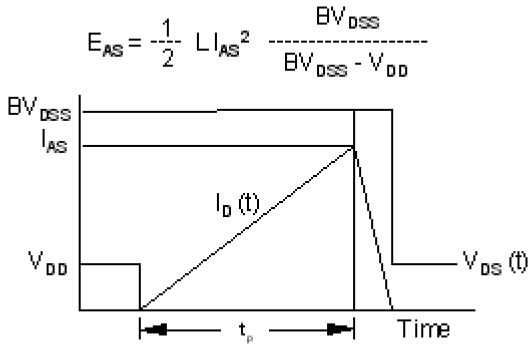
Resistive Switching Test Circuit & Waveforms



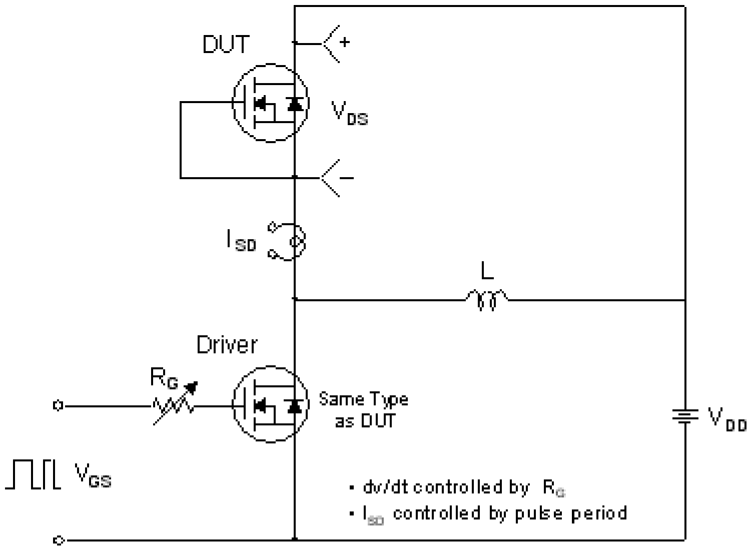


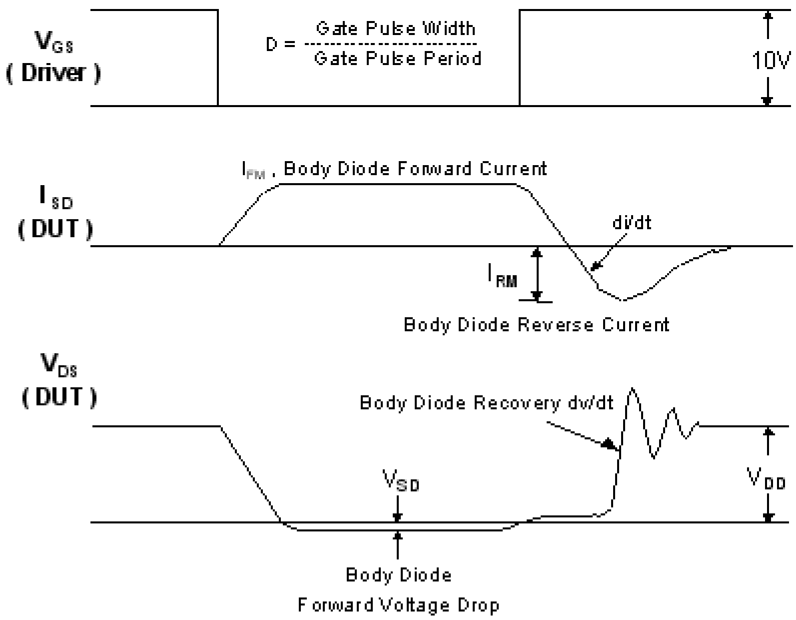
Unclamped Inductive Switching Test Circuit & Waveforms





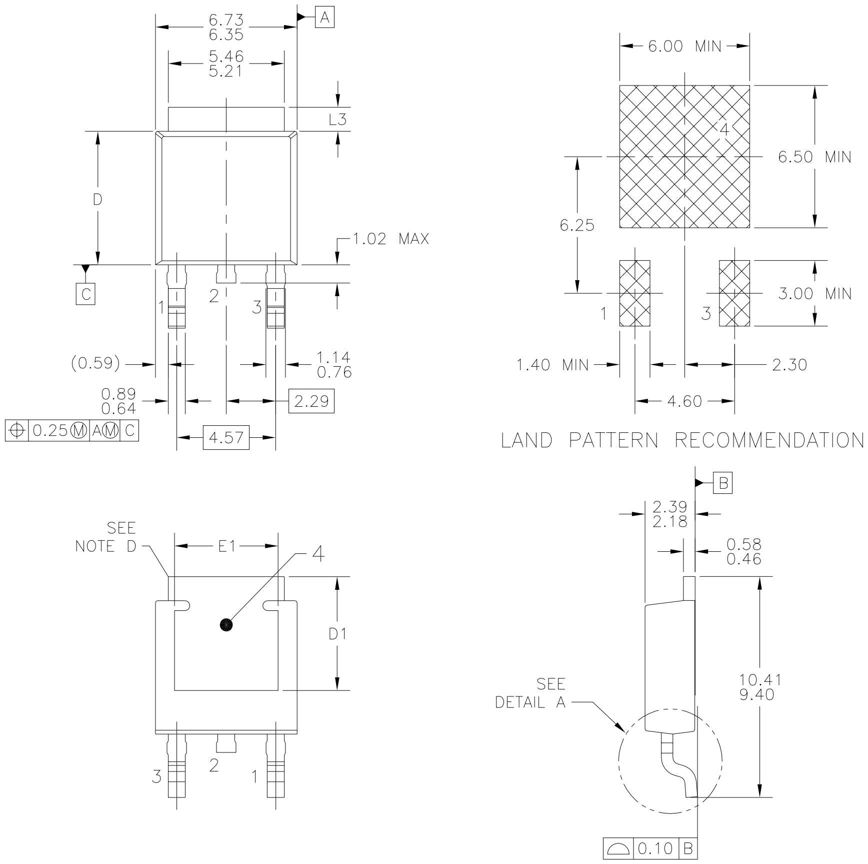
Peak Diode Recovery dv/dt Test Circuit & Waveforms

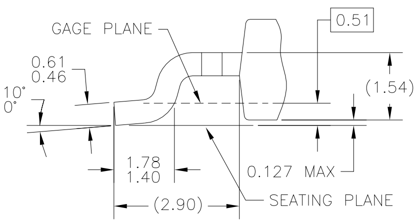




Mechanical Dimensions

D-PAK





DETAIL A
(ROTATED -90°)
SCALE: 12X

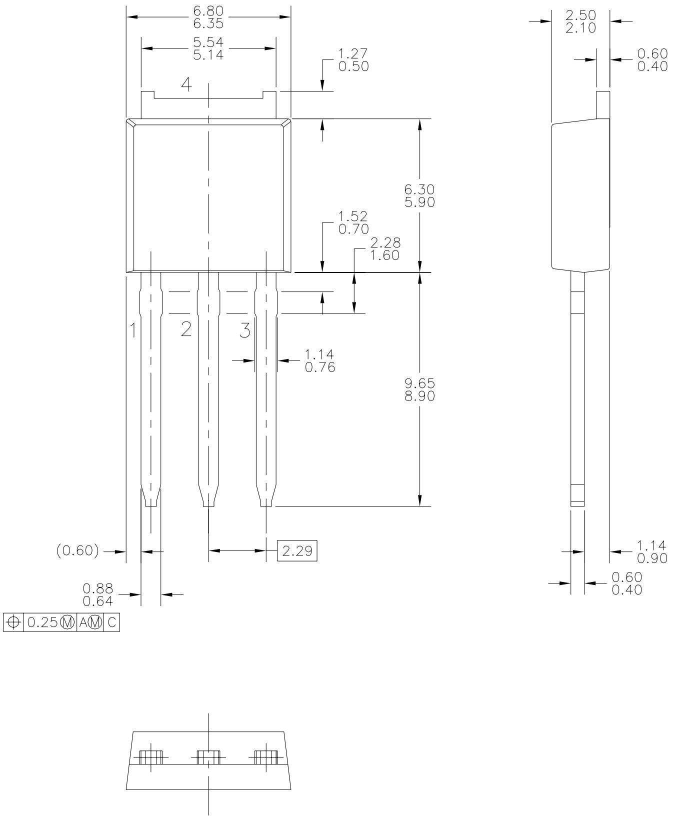
NOTES: UNLESS OTHERWISE SPECIFIED
A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION AA	OPTION AB
L3	0.89-1.27	1.52-2.03
D	5.97-6.22	5.33-5.59
E1	4.32 MIN	3.81 MIN
D1	5.21 MIN	4.57 MIN

F) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Mechanical Dimensions

I-PAK



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